10-18-00 A

NEW UTILITY PATENT APPLICATION TRANSMITTAL	DOCKET NO. END919960138US2 IEN-10-5202-C1
	TOTAL PAGES IN THIS SUBMISSION 3

TO THE ASSISTANT COMMISSIONER FOR PATENTS
Box Patent Application
Washington, D.C. 20231

Transmitted herewith for filing under 35 USC 111(a) and 37 CFR 1.53(b) is a new utility patent application for an invention entitled:

TWO SIGNAL ONE POWER PLANE CIRCUIT BOARD

and invented by:

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ROSS W. KEESLER	IRV MEMIS	WILLIAM E. WILSON
JOHN M. LAUFFER	JIM P. PAOLETTI	

If a CONTINUATION APPLICATION, ***check appropriate box and supply the requisite information:***
☒ **Continuation** ☐ **Divisional** ☐ **Continuation -in -part (CIP)**
in prior application No.: 09/203,956

Enclosed are:

APPLICATION ELEMENTS

1. ☐ Filing fee as calculated and transmitted as described below

2. ☒ Specification having **15** pages and including the following:
   - a. ☒ Descriptive Title of the Invention
   - b. ☐ Cross References to Related Applications *(if applicable)*
   - c. ☐ Statement Regarding Federally-sponsored Research/Development *(if applicable)*
   - d. ☐ Reference to Microfiche Appendix *(if applicable)*
   - e. ☒ Background of the Invention
   - f. ☒ Brief Summary of the Invention
   - g. ☒ Brief Description of the Drawings *(if drawings filed)*
   - h. ☒ Detailed Description
   - i. ☒ Claim(s) as Classified Below
   - j. ☒ Abstract of the Disclosure

3. ☒ Drawing(s) *(when necessary as prescribed by 35 USC 113)*
   - a. ☐ Formal
   - b. ☐ Informal
   - Number of Sheets **3**

4. ☒ Oath or Declaration
   - a. ☐ Newly executed *(original or copy)* ☐ Unexecuted
   - b. ☒ Copy from a prior application (37 CFR 1.63(d)) *(for continuation/divisional application only)*
   - c. ☒ With Power of Attorney
     ☐ Without Power of Attorney

NEW UTILITY PATENT APPLICATION TRANSMITTAL	DOCKET NO. END919960138US2 IEN-10-5202-C1
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Application Elements (Continued)

5. ☒ Incorporation by Reference (*usable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ☐ Computer Program in Microfiche (*Appendix)*

7. ☐ Nucleotide and/or Amino Acid Sequence Submission (*if applicable, all must be included)*
   a. ☐ Paper Copy
   b. ☐ Computer Readable Copy (*identical to computer copy)*
   c. ☐ Statement Verifying Identical Paper and Computer Readable Copy

Accompanying Application Parts

8. ☐ Assignment Papers (*cover sheet & document(s))*

9. ☐ 37 CFR 3.73(B) Statement *(when there is an assignee)*

10. ☐ English Translation Document *(if applicable)*

11. ☒ Information Disclosure Statement/PTO-1449 ☐ Copies of IDS Citations

12. ☒ Preliminary Amendment

13. ☒ Return Receipt Postcard

14. ☒ Certificate of Mailing
   ☐ First Class ☒ Express Mail (*Specify Label No.):* EL 675559378US

15. ☐ Small Entity Statement(s)
   ☐ Statement filed in prior application; Status still proper and desired.

16. ☐ Additional Enclosures *(please identify below):*

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FEE CALCULATION AND TRANSMITTAL

CLAIMS AS FILED

1) For	2) Number Filed	3) Number Extra	Rate	Additional Fee
TOTAL CLAIMS (37 CFR 1 16(c))	14 -20=	-0 -	X$18.00	$ 0.00
INDEPENDENT CLAIMS (37 CFR 1.16(c))	3 - 3 =	- 0 -	X $80.00	$ 80.00
First Pres. of Multiple Dep. Claims		= 0		$ 0.00
Basic Fee		= 0		$710.00
			TOTAL	$710.00

☐ A check in the amount of _____ to cover the filing fee is enclosed.

☒ The Commissioner is hereby authorized to charge and credit Deposit Account No. 09-0457 as described below. A duplicate copy of this sheet is enclosed.

- ☒ Charge the amount of $710.00 as filing fee.
- ☒ Credit any overpayment or any deficiency.
- ☒ Charge any additional filing fees required under 37 CFR 1.16 and 1.17.

Respectfully submitted,

Date: 10-16-00

By: _____

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of Fallon et al	:	
Ser. No. To be assigned	:	Art Unit: To be assigned
Filed: Herewith	:	Examiner: To be assigned
Title: **TWO SIGNAL ONE POWER PLANE CIRCUIT BOARD**	:	

Atty. Docket No. END919960138US2 (IEN-10-5202-C1)

PRELIMINARY AMENDMENT

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Please amend the above entitled application as follows:

In the specification:

On page 1, following the title, insert the following:

--Cross Reference to Related Application

This application is a continuation of patent application serial number 09/203,956, filed December 2, 1998.--

Page 3, line 24, after "a" change "boarder" to --border--;

Page 4, line 11, after "the", second occurrence", change "line 2-2" to --line 2A-2A--;

Page 9, line 9, after "a" change "boarder" to --border--; same page, line 12, after "the", first occurrence, change "boarder" to --border--.

In the claims:

Cancel claims 10-15.

REMARKS

Applicants are submitting this preliminary amendment to cancel claims 10-15 which have been allowed in the parent patent case. In addition, various typographical errors in the specification have been corrected to conform it to the parent application.

Respectfully submitted,

Date: 10-16-00

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APPLICATION

FOR

UNITED STATES LETTERS PATENT

APPLICANT NAME: Fallon et al

TITLE: TWO SIGNAL ONE POWER PLANE CIRCUIT BOARD

DOCKET NO. END919990138US2

INTERNATIONAL BUSINESS MACHINES CORPORATION

TWO SIGNAL ONE POWER PLANE CIRCUIT BOARD

Background of the Invention

This invention relates generally to the formation of circuit boards or cards or the like, and more particularly to the formation of circuit boards or cards having 2 signal planes and one power plane (2S/1P) wherein the power plane is sandwiched between two layers of photopatternable dielectric material and on which layers of circuitry for the signal planes is disposed.

Background Information

In certain conventional circuit board configurations, the circuit board cross-section includes non-photopatternable dielectric, such as FR4 which is epoxy impregnated fiberglass, and one or more layers of copper. Vias and plated through holes are mechanically or laser drilled in the dielectric material. This requires precise alignment drilling with each hole being drilled idefinately and sequentially. Moreover, in some instances it is necessary that there be an isolation border around the edge of the card or board to prevent the power plane from being exposed at the edge. Isolation borders are also created within a card or board to allow separate voltage areas on the same plane. Isolation borders are created by etching away the copper, which exposes the FR4 material therebelow. The exposed FR4 material isolates two adjacent areas of copper, which by design should not be in contact with each other. The isolation border is also used around the edge of the board to prevent exposed copper on the edges from abutting together in the card or board profile operation. The same technique is used to display text on the board, such as part numbers, etc.

While photoimageable material has been used on one side of a metal substrate, various processing difficulties are encountered when using photoimageable material to form a 2S/1P board, with the photoimageable material on both sides of the metal power plane. In a process that sandwiches a preformed metal power plane with photoimageable dielectric polymers as the dielectric material on which circuit traces are to be formed, isolation borders cannot be formed in the same way as with the non-photopatternable FR4. If the same process were used after the copper is etched away, the parts of the panel would be isolated and would literally fall apart since there is no remaining material to hold them together.

It is therefore a principal object of the present invention to provide a process in which layers of photoimageable dielectric material are used on opposite sides of a metal layer forming a power plane and on which circuit traces are formed and in which vias and plated through holes are formed. In one aspect a technique is provided wherein an isolation border can be formed in the power plane without the panel falling apart.

Summary of the Invention

According to the present invention, a method of forming a printed circuit board or circuit card is provided wherein there is metal layer which serves as a power plane sandwiched between a pair of photoimageable dielectric layers, and wherein photoformed metal filled vias and photoformed plated through holes are formed in the photopatternable material, and signal circuitry is formed on the surfaces of each of the dielectric materials and connected to the vias and plated through holes. In one embodiment, a border around the board or card is provided wherein said metal layer terminates a distance spaced from the edge of one of the dielectric layers.

A border can also be used within a card or board to isolate separate voltages on the same plane. The method includes the steps of providing a layer of metal preferably copper foil with clearance holes. A first layer of photoimageable dielectric curable material is disposed on one side of the foil, and a second layer of photoimageable curable dielectric material is disposed on the other side of said layer of material. Preferably, the photoimageable dielectric material is an epoxy-based resin.

Both the first and second layers of the curable photoimageable material are photopatterned in a pre-selected pattern on each side. (If a border is to be formed, the first layer of photoimageable material includes a border pattern, and the pattern on the second layer of photoimageable material does not include the border pattern.) The patterns are developed on the first and second layers of the photoimageable material to reveal the metal layer through vias and in the case of a border to reveal the metal at the border in the developed patterns. At the clearance holes in the metal layer, through holes have been developed where holes were patterned in both dielectric layers. Thereafter, the surface of each of the photoimageable material, vias and through holes are metalized by the use of photolithographic techniques and preferably through additive copper plating. If a ~~border~~ border is present, the metal surrounding the borders revealed through the first layer is etched to thereby provide a substrate which has an edge defined by the second layer of photoimageable material extending beyond the edge of the metal layer. This etching is preferably done by protecting the remainder of the circuitry by the use of photoresist and utilizing photolithographic techniques. When such technique is used, the photoresist is thereafter removed, thereby leaving a circuit board or card having metalization on both sides, vias

extending from both sides to the metal layer in the center, plated through holes connecting the two outer circuitized metal layers, and in the case of forming a board with the metal removed to form a border supported by one of the patternable dielectric materials which remain undeveloped.

Description of the Drawings

Figure 1 is a plan view, somewhat schematic, showing the various cards or boards formed on a panel during processing;

Figures 2a-2k are sectional views taken substantially along the plane designated by the line 2A-2A of Figure 1, showing the formation of a circuit board in its various stages of manufacturing.

Description of the Preferred Embodiment

Referring now to the drawings, Figure 1 shows a very schematic representation of a panel used to form a plurality of circuit cards or boards thereon when the cards, boards or sections of cards or boards are required to be electrically separated, i.e., there can be no physical contact in the power plane between the various cards or boards being formed. As shown in Figure 1, panel 10 has a plurality of circuit cards designated by the reference character 12 formed thereon, and the various cards 12 are separated by borders 14 which extend completely around each of the cards 12. Borders 16 are borders that provide an electrical separation within a card. The term "cards" or "circuit cards" is used herein to designate circuitized substrates which can be used as chip carriers, or circuit boards for the mounting of components as well as chips. The formation of the cards 12 is shown in the various stages thereof in Figures 2a-2k starting with a metal layer which will form the power plane and progressing through the various steps to form a final circuitized card or board

with a border therearound free of the metal which forms the power plane.

Referring now to Figure 2a, a metal layer 20 is shown which in one preferred embodiment is copper in the form of a 1-oz. copper foil, although other sizes of copper foil could be used; e.g., 1/2-oz. copper foil. However, 1-oz. copper foil is one standard material conventionally used for a power plane. It is contemplated that the metal layer should be from about 0.7 mil to about 2.8 mils thick. Formation will be described in forming a circuit card which has a 1P/2S configuration, i.e., 1 power plane and 2 signal planes.

In many instances, plated through holes are required which extend from the circuitry on the exposed surface of one layer of dielectric to the circuitry on the exposed surface of the other dielectric material. In such a case, through holes, one of which is shown at 22, are formed in the copper foil 20. These can be formed either by mechanical drilling or by etching. One technique for etching is by the use of photolithographic process wherein the location of each of the holes is patterned and developed in photoresist which is coated onto both surfaces of the copper, and the holes etched through the copper by an etchant such as cupric chloride ($CuCl_2$). The photo resist is then stripped. This process is well known in the art.

A first layer of photoimageable dielectric material 24 is coated onto one side of the copper foil 20, a second layer of a photoimageable dielectric material 26 is coated on the opposite side of the copper foil 20, and the dielectric material fills in the through hole 22 as shown as 28. Each layer of dielectric material is preferably between 2 mils and 4 mils thick. A particularly useful photoimageable material is an epoxy-based material of the type described in U.S. Patent No. 5,026,624, entitled "Composition for Photoimaging",

commonly assigned, which is incorporated herein by reference. As shown in Figure 2b, this material is photoimaged or photopatterned, developed to reveal the desired pattern, and thereafter cured to provide a dielectric substrate on which metal circuit traces such as plated copper can be formed for forming the circuit board. The dielectric material may be curtain coated as described in said patent No. 5,026,624, or it can contain a thixotrope and be screen applied as described in U.S. Patent No. 5,300,402. The material may also be applied as a dry film. A technique for forming a dry film is as follows:

The photoimageable dielectric composition is prepared having a solids content of from about 86.5 to 89%, such solids comprising: about 27.44% PKHC a phenoxy resin; 41.16% of Epirez 5183 a tetrabromobisphenol A; 22.88% of Epirez SU-8, an octafunctional epoxy bisphenol A formaldehyde novolac resin, 4.85% UVE 1014 photoinitiator; 0.07% ethylviolet dye; 0.03% Fc 430 a fluorinated polyether nonionic surfactant from 3M Company; 3.85% Aerosil 380, an amorphous silicon dioxide from Degussa; to provide the solid content. Solvent was present from about 11 to 13.5% of the total photoimageable dielectric composition. The photoimageable dielectric composition is coated onto a 1.42 mil thick segment of polyethylene terephthalate designated Mylar D a segment of polyethylene terephthalate designated Mylar D a polyester layer from DuPont. The photoimageable dielectric composition is allowed to dry to provide a 2.8 mil thick photoimageable dielectric film on the polyethylene terephthalate backing.

The particular material 24 and 26 as described in said Patents No. 5,026,624 and 5,300,402 is negative acting photodielectric. Hence, those areas which are exposed to actinic radiation, in this case UV light, will not be developed (i.e., will remain) when the material is developed

in developer, and areas which are not exposed will be removed, i.e., developed out. Masks are applied over both the photoresist 24 and 26 having those areas which are to be developed blanked out, and the remainder of the dielectric material 24 and 26 exposed to UV light. The preferred agent for developing this material is propylene carbonate. As shown in Figure 2c, this will provide openings 32 which extend to the surface of the copper foil 20 and openings 34 on the photoresist 24 which will reveal the foil 20 thereunder which will form the border, and openings 36 which are smaller in diameter than the openings 32 in the copper foil 20 which will thus allow for a plated through hole. Following the development, the remaining dielectric material 24 and 26 is given a UV bump and then cured at between 150°C and 190°C as described in said Patent No. 5,026,624. The developing and curing is described in detail in said U.S. Patent No. 5,026,624. The dielectric material can be sufficiently toughened to form a base on which electrical circuitry can be deposited or formed. Following this, the entire surface is treated by vaporous blasting and optional desmearing, and then seeded for copper plating, preferably with palladium 38, so as to provide for electroless copper plating as is well known in the art. This stage of manufacture is shown in Figure 2c.

Both sides of the product at this point are coated with photoresist 40, as shown in Figure 2d, preferably the resist is DuPont Resiston T168, which is a negative acting photoresist. The photoresist is then exposed everywhere except where copper plating is to take place and is developed. The resist is preferably developed with propylene carbonate as is well known and will form openings 42 through the photoresist 40 at places where the copper plating is to take place. The openings will be located above the layers 24 and 26 where circuit traces are to be formed, where vias are to be

formed and where plated through holes are to be formed. This stage of manufacture is shown in Figure 2e.

Following this, copper is electrolessly plated according to well-known techniques onto the exposed areas through the openings 42 in the photoresist 40 as shown in Figure 2f to form circuit tracers 44 on dielectric material 24 and 26, and blind vias 46 extending through dielectric material 24 and 26 in contact with copper layer 10 and plated through holes 48. Following this, optionally the surfaces can be planarized, although this is often not required.

Following the electroless plating, the photoresist 40 is stripped as shown in Figure 2g by propylene carbonate at elevated temperatures so as to provide circuitry 44, vias 46 and plated through holes 48. Developing of the photoresist also reveals the copper 20 beneath the photoresist 24 in openings 34 therein. The copper 20 is not revealed on the opposite side through photoresist 26. At this stage, the remaining palladium seed 38 on which plating has not occurred is stripped, preferably in a cyanide bath.

Following the stripping of the palladium seed, another coating of photoresist 50 is applied to both sides of the part shown in Figure 2h. Preferably, this photoresist is negative acting MI photoresist sold by the MacDermid Company. The photoresist 50 overlying the photopatternable material 24 is exposed everywhere except at the opening 34 and developed to provide an opening 52 communicating with the opening 34. This can be developed by the use of sodium carbonate. This is shown in Figure 2i.

The copper revealed under the opening 34 is then etched, preferably using a cupric chloride solution which will provide the part as shown in Figure 2j.

The remainder of the photoresist 50 is then stripped with NaOH, which will result in the part shown in Figure 2k. As

can be seen, the copper foil 20 terminates at the outer edge of the photopatternable material 24, whereas the outer edge of the photopatternable material 26 extends beyond the copper 24. Thus, referring again to Figure 1, the entire panel is held together by the bottom photopatternable material 26 even though a border has been created in the top photopatternable material 24 and in the copper 20 therearound, thus preserving the integrity of the entire panel 10.

If a boarder is not required, i.e. if the Cu sheet 20 can be maintained as a unit and extended up to the edge of the board, the steps in the process described above relating to forming the boarder can be omitted. Thus, the opening 34 is not formed, and the photopatterning and plating will take place as shown in Figures 2c through 2g which will represent the final product, since the steps shown in Figures 2h through 2k are unnecessary.

Accordingly, the preferred embodiment of the present invention has been described. With the foregoing description in mind, however, it is understood that this description is made only by way of example, that the invention is not limited to the particular embodiments described herein, and that various rearrangements, modifications, and substitutions may be implemented without departing from the true spirit of the invention as hereinafter claimed.

What is claimed is:

1. A method of forming a printed circuit card wherein there is a metal layer sandwiched between a pair of dielectric layers and wherein there is a border therearound, in which said metal layer terminates at a distance spaced from the edge of one of the dielectric layers comprising the steps of;

providing a layer of metal having opposite sides;

providing first and second layers of photoimageable, curable dielectric material on the opposite sides of said layer of metal;

photopatterning said first and second layers of said curable photoimageable material in a pre-selected pattern, the pattern on said first layer of photoimageable material including a border pattern, and the pattern on said second layer of said photoimageable material being free of a border pattern;

thereafter developing said patterns on said first and second layers of said photoimageable material to reveal portions of said metal layer through vias and said border in the developed pattern;

thereafter metalizing each of said first and said second layers to form circuitry on said first and second layers of said photoimageable material and vias in said first and second layers of photoimageable material with photolithographic techniques and etching the metal exposed at said border through said first layer to thereby provide a substrate which has an edge defined by the second layer of said photoimageable material extending beyond the edge of said metal layer.

2. The invention as defined in claim 1 further characterized by photoforming a hole extending through both of

said layers of dielectric material and said metal layer, and depositing metal in said hole.

3. The invention as defined in claim 1 wherein said metal layer between said layers of dielectric material is copper.

4. The invention as defined in claim 1 wherein said photoimageable material is an epoxy-based resin.

5. The invention as defined in claim 1 wherein the metal exposed at said border is etched following the metalization of the first and second layers.

6. The invention as defined in claim 3 wherein the metalization of the first and second layers is accomplished by electroless plating of copper.

7. The invention as defined in claim 1 wherein a plurality of circuit boards are formed on a panel.

8. The invention as defined in claim 1 wherein said first and second layers of photoimageable material are applied as a dry film material.

9. The invention as defined in claim 2 further characterized by forming an opening in said metal layer prior to providing the first and second layers of photoimageable material, filling said opening with said photoimageable material, forming a hole in the photoimageable material through the metal layer opening, and providing metal in said hole in said photoimageable material filling said opening.

10. A printed circuit card comprising a metal layer sandwiched between a pair of dielectric layers, said dielectric layers each being formed of a photoimaged cured dielectric material and each having an outer edge, a border surrounding said circuit card, said border being comprised of said metal layer terminating at a distance spaced from the edge of one of the dielectric layers and adjacent the edge of said other dielectric layer;

metalization on each of said first and said second layers forming circuitry on said first and second layers of said photoimageable material, and metal filled vias in said first and second layers of photoimageable material connected to said circuitry and to said metal layer.

11. The invention as defined in claim 10 further characterized by a plated through hole extending through each layer of dielectric material and through the metal layer.

12. The invention as defined in claim 11 wherein said plated through hole is electrically connected to the circuitry on both dielectric materials.

13. The invention as defined in claim 10 wherein a plurality of circuit boards comprise a panel connected by the borders at said one dielectric layer of material.

14. The invention as defined in claim 10 wherein the layer of metal is copper.

15. The invention as defined in claim 10 wherein the circuitry is copper.

16. A method of forming a printed circuit card comprising the steps of,

providing a layer of metal having opposite sides,

forming at least one opening through said layer of metal,

provide first and second layers of photoimageable material on opposite sides of said layer of metal,

photopatterning and developing said first and second layers of said photoimageable material to form an opening extending through both layers of said photoimageable material and said at least one opening in said metal layer and which openings in said photoimageable layers are smaller than the opening in said layer of metal, forming and at least one via in at least one layer of photoimageable material that terminates at said layer of metal, circuitizing the exposed surface of each of said layers of photoimageable material with circuitry and depositing metal in said at least one hole in said photoimageable material and in said at least one via.

17. The invention as defined in claim 16 wherein said photoimageable material is deposited as a dry film.

18. The invention as defined in claim 16 wherein said circuitry is formed by additive plating.

19. A printed circuit card comprising a metal layer sandwiched between a pair of dielectric layers, said dielectric layers each being formed of a photoimaged cured dielectric material,

metalization on each of said first and said second layers forming circuitry on said first and second layers of said photoimageable material, and metal filled vias in at least said first layer of photoimageable material connected to

said circuitry and to said metal layer and an opening in said metal layer and in said first and second layers of photoimageable material, said opening being metallized to connect at least a portion of the circuitry on said first layer with a portion of circuitry on said second layer without contacting said metal layer.

20. The invention as defined in claim 19 wherein said holes and vias in said dielectric material are photoformed.

TWO SIGNAL ONE POWER PLANE CIRCUIT BOARD

Abstract of the Disclosure

A method of forming a printed circuit board or circuit card is provided with a metal layer which serves as a power plane sandwiched between a pair of photoimageable dielectric layers. Photoformed metal filled vias and photoformed plated through holes are in the photopatternable material, and signal circuitry is on the surfaces of each of the dielectric materials and connected to the vias and plated through holes. A border may be around the board or card including a metal layer terminating in from the edge of one of the dielectric layers. A copper foil is provided with clearance holes. First and second layers of photoimageable curable dielectric material is disposed on opposite sides of the copper which are photoimageable material. The patterns are developed on the first and second layers of the photoimageable material to reveal the metal layer through vias. At the clearance holes in the copper, through holes are developed where holes were patterned in both dielectric layers. Thereafter, the surfaces of the photoimageable material, vias and through holes are metalized by copper plating. This is preferably done by protecting the remainder of the circuitry with photoresist and utilizing photolithographic techniques. The photoresist is thereafter removed, leaving a circuit board or card having metalization on both sides, vias extending from both sides to the copper layer in the center, plated through holes connecting the two outer circuitized copper layers.

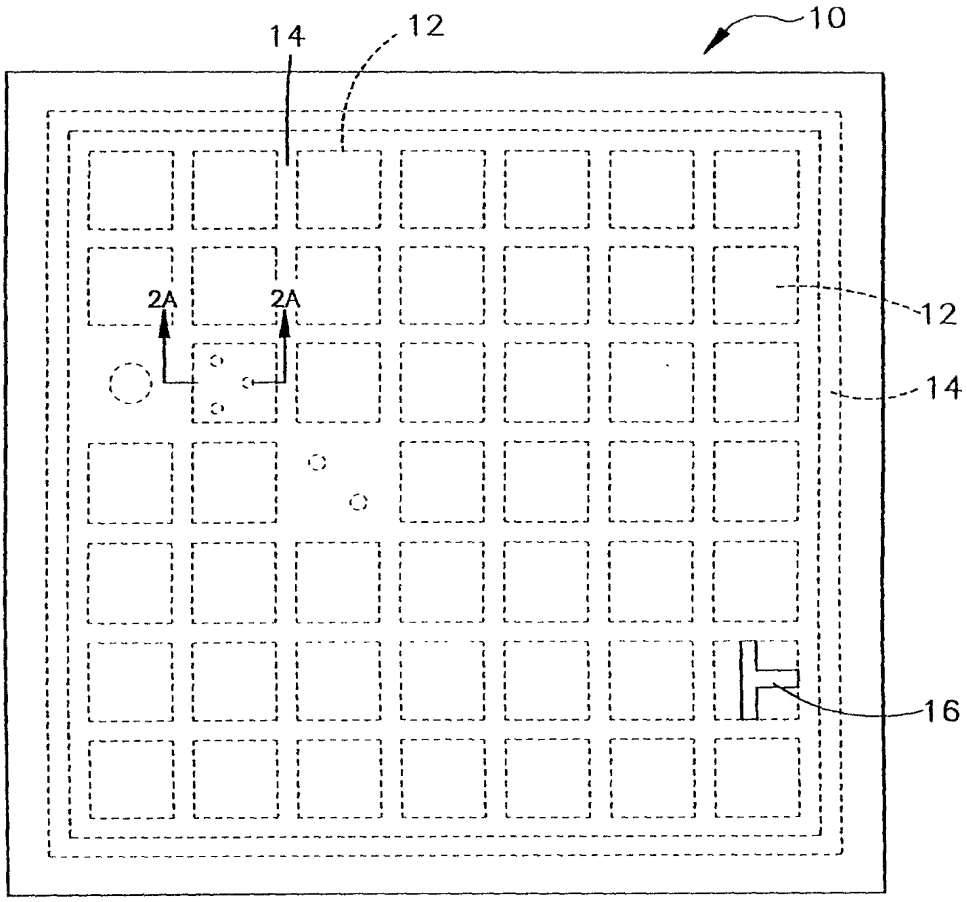


Fig.1

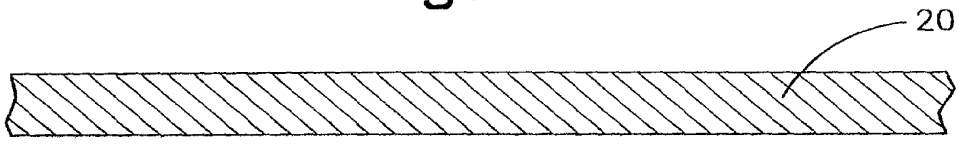


Fig.2A

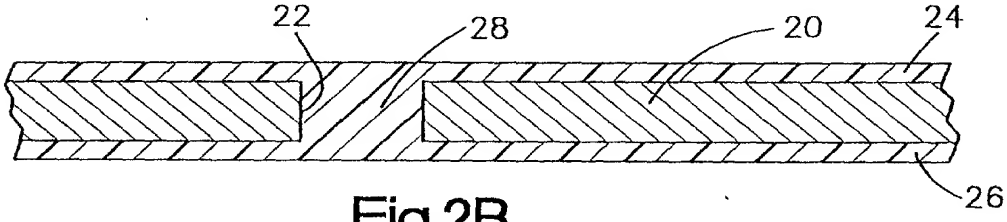


Fig.2B

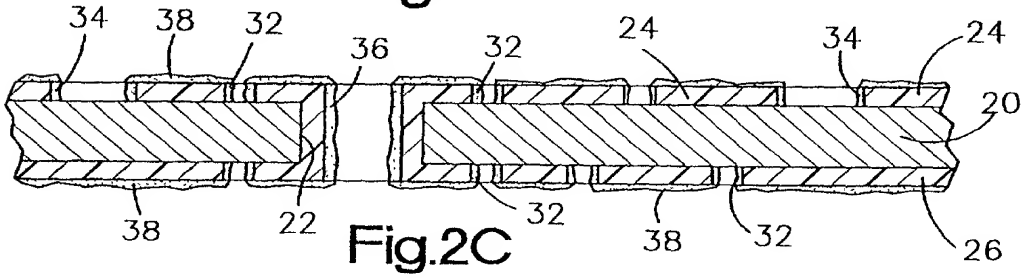


Fig.2C

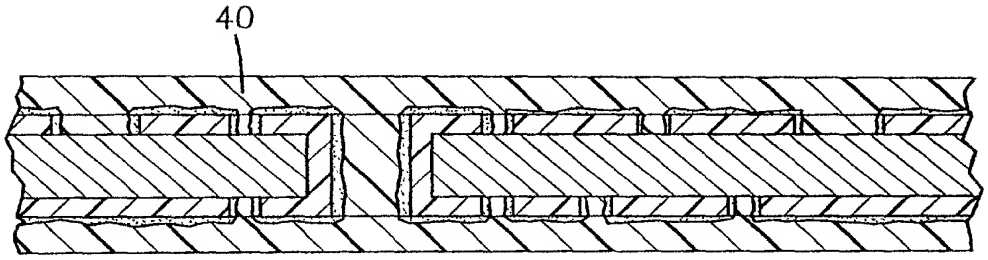


Fig.2d

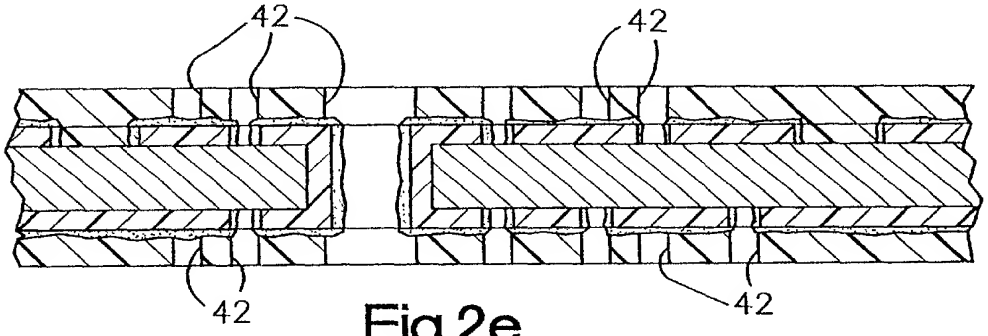


Fig.2e

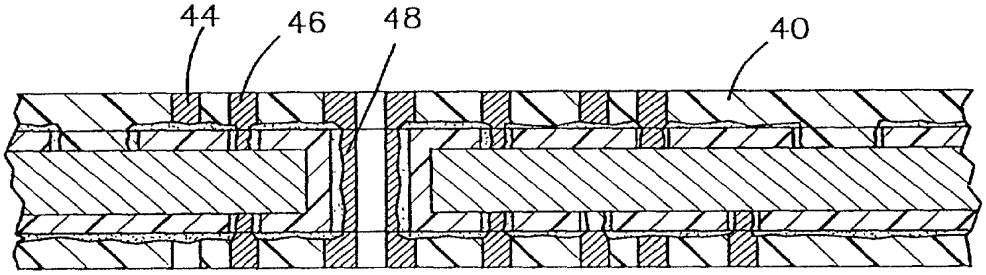


Fig.2f

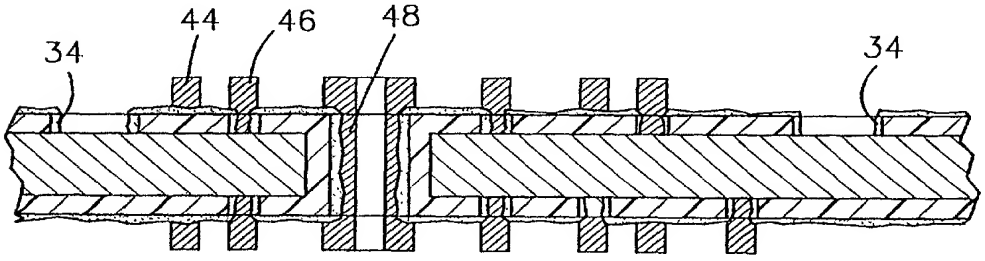


Fig.2g

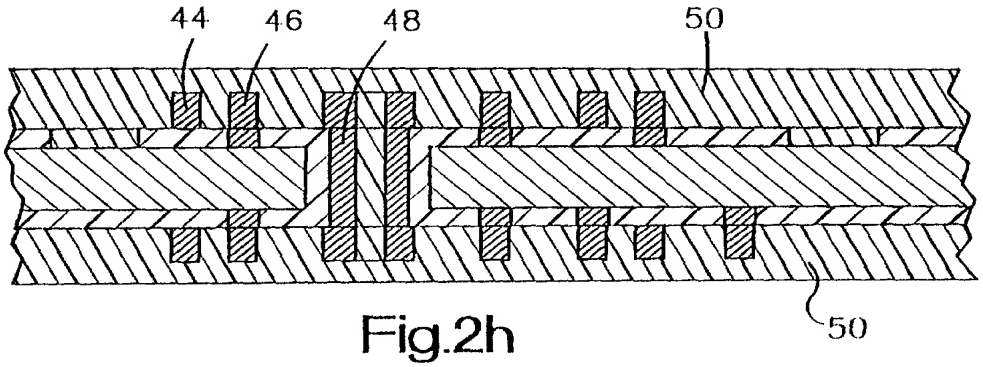


Fig.2h

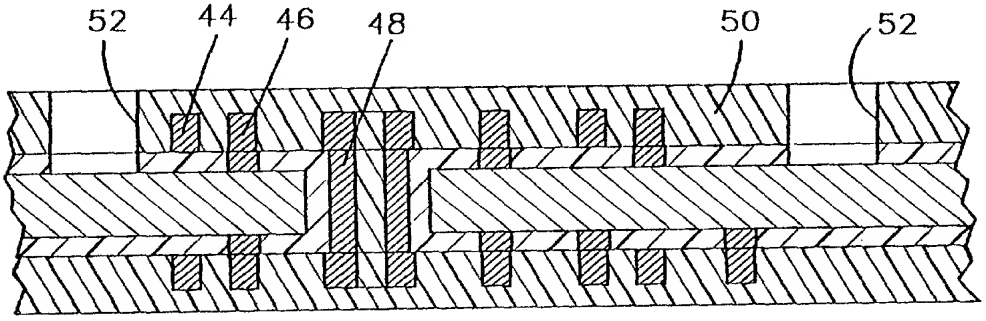
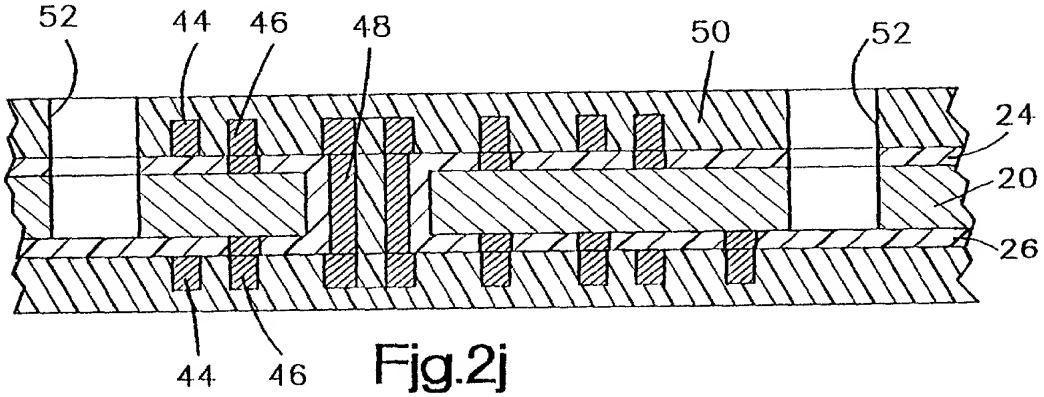
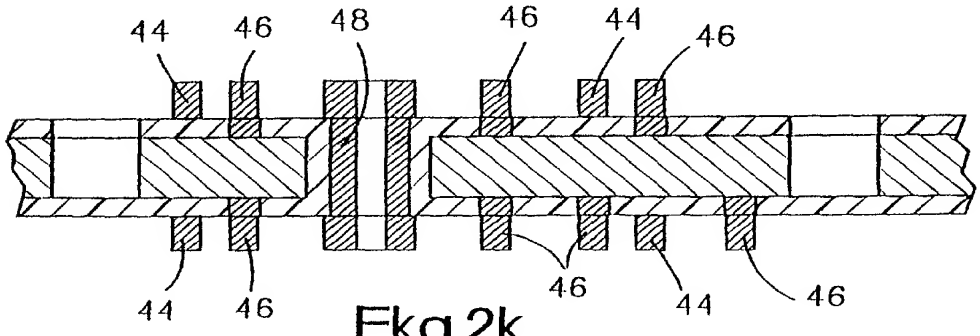


Fig.2i



Fjg.2j



Fkg.2k

PATENT
DOCKET NUMBER: EN9-96-138 (21325/00280)

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled

TWO SIGNAL ONE POWER PLANE CIRCUIT BOARD

the specification of which: (check one)

☒ is attached hereto.

☐ was filed on _____
under Attorney's Docket Number _____
as Application Serial No. _____
and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 CFR 1.56.

I hereby claim the benefit of foreign priority under 35 USC 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):			Priority Claimed
_____	_____	_____	___ Yes ___ No
(Number)	(Country)	(Day/Month/Year)	

I hereby claim the benefit of United States priority under 35 USC 120 of any United States application(s) listed bellow and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of 35 USC 112, I acknowledge the duty to disclose information material to the patentability of this application as defined in 37 CFR 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

_____	_____	_____
(Application Serial #)	(Filing Date)	(Status)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 USC 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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